

General Description

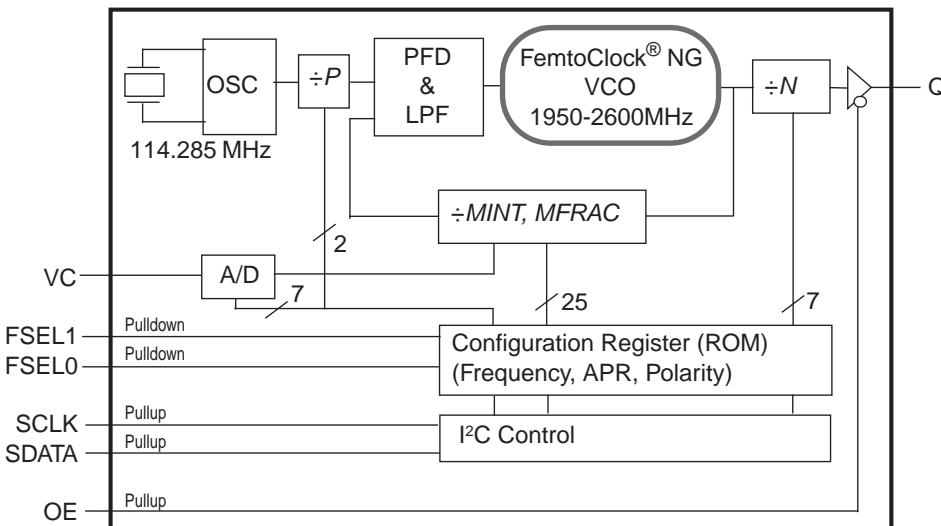
The 8N0QV01 is a Quad-Frequency Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT's Fourth Generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead ceramic 5mm x 7mm x 1.55mm package.

Besides the four default power-up frequencies set by the FSEL0 and FSEL1 pins, the 8N0QV01 can be programmed via the I²C interface to any output clock frequency between 15.476MHz to 260MHz to a very high degree of precision with a frequency step size of 435.9Hz ÷ N (N: PLL post divider). Since the FSEL0 and FSEL1 pins are mapped to four independent PLL, P, M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

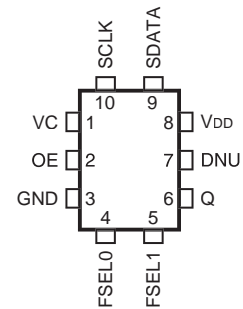
Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 260MHz
- Four power-up default frequencies (see part number order codes), re-programmable by I²C
- I²C programming interface for the output clock frequency, APR and internal PLL control registers
- Frequency programming resolution is 435.9Hz ÷ N
- Absolute pull-range (APR) programmable from ±2.5 to ±727.5ppm
- One 2.5V, 3.3V LVCMOS clock output
- Two control inputs for the power-up default frequency
- LVCMOS/LVTTL compatible control inputs
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.635ps (typical)
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): 0.850ps (typical)
- 2.5V or 3.3V supply voltage modes
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



IDT8N0QV01 Rev H
10-lead ceramic 5mm x 7mm x 1.55mm
package body
CD Package
Top View

Package Outline and Package Dimensions

